

WHAT IS CLAIMED IS:

1 1. A data processing method, comprising:
 2 receiving one or more clock-data streams;
 3 dividing said one or more clock-data streams into at least one clock stream
 4 and at least one data stream; and
 5 synchronizing each of said at least one data stream to a common clocking
 6 domain for processing.

1 2. A method in accordance with claim 1, including multiplexing a plurality
 2 of said at least one data stream for processing by a framer array, said framer array
 3 being provided offset a data path of said at least one data stream.

1 3. A method in accordance with claim 2, further comprising aligning
 2 octets of said at least one data stream onto a multiplexed bus synchronized to said
 3 common clocking domain.

1 4. A method in accordance with claim 3, further comprising:
 2 demultiplexing said plurality of at least one data stream and recombining said
 3 at least one data stream and said at least one clock stream.

1 5. A method according to claim 4, said at least one data stream
 2 comprising status and control information.

1 6. A data processing system, comprising:
 2 means for receiving a plurality of asynchronous combined clock-data streams;
 3 means for dividing said clock-data streams into component clock and data
 4 streams;
 5 means for processing said data streams in a common clock domain; and
 6 means for recombining said component clock and data streams.

1 7. A data processing system according to claim 6, said processing means

2 including a common bus onto which said component data streams are multiplexed.

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1 8. A data processing system according to claim 7, said processing means
2 including a framer state machine offset from said common bus adapted to align
3 octets of said component data streams onto said common bus.

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1 9. A data processing system according to claim 8, said processing means
2 including a framer state machine adapted to store a context of a last data stream
3 processed and load a context of a current data stream.

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1 10. A system, comprising:
2 a plurality of clock paths adapted to extract clocks from a plurality of clock-
3 data streams;
4 a plurality of data paths adapted to receive data portions of said clock-data
5 streams and provide said data portions onto a common bus in a common clock
6 domain; and
7 a framer unit offset from said common bus and adapted to load and store a
8 context for said data portions.

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1 11. A system according to claim 10, said framer unit further adapted to
2 identify a start of frames of said data portions.

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1 12. A system according to claim 11, including a plurality of synchronizers
2 adapted to synchronize each of said plurality of data paths to said common bus.

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1 13. A system according to claim 12, including a plurality of serial-to-parallel
2 converters coupled to said plurality of synchronizers.

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1 14. A system according to claim 13, wherein outputs of said serial-to-
2 parallel converters are provided to a multiplexer.

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1 15. A system according to claim 14, wherein outputs of said multiplexer

